May 2000
Revised December 2005

FSA266 • NC7WB66

Low Voltage Dual SPST Normally Open Analog Switch or 2-Bit Bus Switch

General Description

The FSA266 or NC7WB66 is an ultra high-speed (UHS) dual single-pole/single-throw (SPST) analog switch or 2-bit bus switch. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low On Resistance over a broad V_{CC} range. The device is specified to operate over the 1.65 to 5.5V V_{CC} operating range. The device is organized as a dual switch with independent CMOS compatible switch enable (OE) controls. When OE is HIGH, the switch is ON and Port A is connected to Port B. When OE is LOW, the switch is OPEN and a high-impedance state exists between the two ports. The enable inputs tolerate voltages up to 5.5V independent of the V_{CC} operating range.

Features

- Useful in both analog and digital applications
- Space saving US8 surface mount package
- MicroPak™ Pb-Free leadless package
- Typical 7Ω On Resistance @ 5V V_{CC}
- Broad V_{CC} operating range: 1.65V to 5.5V
- Rail-to-Rail signal handling
- Power down high impedance control inputs
- Control inputs are overvoltage tolerant
- Control inputs are CMOS compatible
- >300 MHz −3dB bandwidth

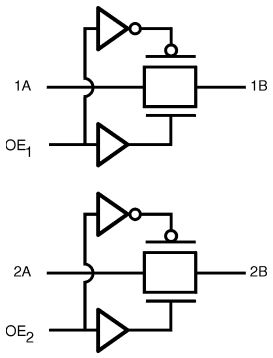
Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
FSA266K8X	MAB08A	WB66	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3K Units on Tape and Reel
FSA266L8X	MAC08A	P4	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5K Units on Tape and Reel
NC7WB66K8X	MAB08A	WB66	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3K Units on Tape and Reel
NC7WB66L8X	MAC08A	P4	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5K Units on Tape and Reel

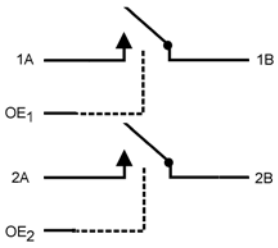
Pb-Free package per JEDEC J-STD-020B.

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Logic Symbol

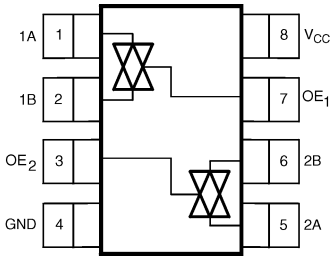


Analog Symbol



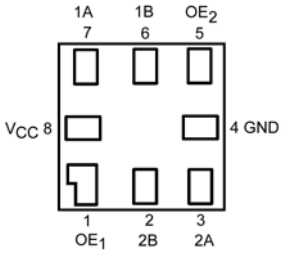
Connection Diagrams

Pin Assignments for US8



(Top View)

Pad Assignments for MicroPak



(Top Through View)

Pin Descriptions

Pin Names	Description
A	Switch Port A
B	Switch Port B
OE	Control Input

Function Table

Switch Enable Input (OE)	Function
L	Disconnect
H	B Connected to A

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to V_{CC} + 0.5V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current	
@ (I_{IK}) V_{IN} < 0V	−50 mA
DC Switch Output Current (I_{OUT})	±128 mA
DC V_{CC} or Ground Current (I_{CC}/I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Junction Lead Temperature	
under Bias (T_J)	+150°C
Junction Lead Temperature (T_L)	
(Soldering, 10 Seconds)	+260°C
Power Dissipation (P_D) @ +85°C	
SC70-6	250 mW

Recommended Operating Conditions (Note 3)

Supply Voltage (V_{CC})	1.65V to 5.5V
Control Input Voltage (V_{IN})	0V to 5.5V
Switch Input Voltage (V_{IN})	0V to V_{CC}
Switch Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
Control Input V_{CC} = 1.65V–2.7V	0 ns/V to 20 ns/V
Control Input V_{CC} = 3.0V–3.6V	0 ns/V to 10 ns/V
Control Input V_{CC} = 4.5V–5.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	250°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95	0.75 V_{CC}			0.75 V_{CC}		V	
		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}			
V_{IL}	LOW Level Input Voltage	1.65 to 1.95			0.25 V_{CC}		0.25V_{CC}	V	
		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}		
I_{IN}	Input Leakage Current	0 to 5.5			±0.1		±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
I_{OFF}	Switch OFF Leakage Current	1.65 to 5.5			±0.1		±1.0	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch On Resistance	4.5		6.0	10.0		10.0	Ω	V_I = 0V, I_O = 30 mA
	(Note 4)			7.0	13.5		13.5		V_I = 2.4V, I_O = −30 mA
				6.0	10.0		10.0		V_I = 4.5V, I_O = −30 mA
		3.0		7.5	15.0		15.0	Ω	V_I = 0V, I_O = 24 mA
				8.5	15.0		15.0		V_I = 3V, I_O = −24 mA
		2.3		9.0	20.0		20.0	Ω	V_I = 0V, I_O = 8 mA
				10.5	20.0		20.0		V_I = 2.3V, I_O = −8 mA
		1.65		12.5	30.0		30.0	Ω	V_I = 0V, I_O = 4 mA
				17.0	30.0		30.0		V_I = 1.65V, I_O = −4 mA
I_{CC}	Quiescent Supply Current	5.5			1.0		10.0	µA	V_{IN} = V_{CC} or GND
	All Channels ON or OFF								I_{OUT} = 0
	Analog Signal Range	V_{CC}	0		V_{CC}	0	V_{CC}	V	
RRange	On Resistance Over	4.5		8.0	15.0		15.0	Ω	I_O = −30 mA, 0 ≤ V_I ≤ V_{CC}
	Signal Range	3.0		15.0	30.0		30.0		I_O = −24 mA, 0 ≤ V_I ≤ V_{CC}
	(Note 4)(Note 5)	2.3		45.0	75.0		75.0		I_O = −8 mA, 0 ≤ V_I ≤ V_{CC}
		1.65		150	275		275		I_O = −4 mA, 0 ≤ V_I ≤ V_{CC}
ΔR_{ON}	On Resistance Match	4.5		0.2				Ω	I_O = −30 mA, V_I = 3.15
	Between Channels	3.0		0.2					I_O = −24 mA, V_I = 2.1
	(Note 4)(Note 7)	2.3		0.5					I_O = −8 mA, V_I = 1.6
		1.65		0.6					I_O = −4 mA, V_I = 1.15
R_{flat}	On Resistance Flatness	4.5		2.5	6.0		6.0		I_O = −30 mA, 0 ≤ V_I ≤ V_{CC}
	(Note 4)(Note 5)(Note 6)	3.0		8.0	17.5		17.5		I_O = −24 mA, 0 ≤ V_I ≤ V_{CC}
		2.3		33.0	60.0		60.0		I_O = −8 mA, 0 ≤ V_I ≤ V_{CC}
		1.65		135	250		250		I_O = −4 mA, 0 ≤ V_I ≤ V_{CC}

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: Guaranteed by design.

Note 6: Flatness is defined as the difference between the minimum and maximum value of ON Resistance over the specified range of conditions.

DC Electrical Characteristics (Continued)

Note 7: $\Delta R_{ON} = R_{ON}$ max − R_{ON} min measured at identical V_{CC}, temperature and voltage levels.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions	Figure Number
			Min	Typ	Max			
t_{PHL}, t_{PLH}	Propagation Delay Bus-to-Bus (Note 8)	4.5 to 5.5		0.35	1.0	ns	V_I = OPEN C_L = 50 pF, RU = RD = 500Ω	Figures 1, 2
		3.0 to 3.6		0.7	1.5			
		2.3 to 2.7		1.1	2.5			
		1.65 to 1.95		2.0	4.0			
t_{PZL}, t_{PZH}	Output Enable Time Turn on Time	4.5 to 5.5	0.8	2.0	3.2	ns	V_I = 0V for t_{PZH} V_I = 2 x V_{CC} for t_{PZL} C_L = 50 pF, RU = RD = 500Ω	Figures 1, 2
		3.0 to 3.6	1.2	2.5	3.9			
		2.3 to 2.7	1.5	3.2	5.6			
		1.65 to 1.95	2.5	5.7	10.0			
t_{PLZ}, t_{PHZ}	Output Disable Time Turn Off Time	4.5 to 5.5	0.8	2.6	4.1	ns	V_I = 0V for t_{PHZ} V_I = 2 x V_{CC} for t_{PLZ} C_L = 50 pF, RU = RD = 500Ω	Figures 1, 2
		3.0 to 3.6	1.5	3.4	5.0			
		2.3 to 2.7	2.0	4.2	6.9			
		1.65 to 1.95	3.0	6.2	10.5			
Q	Charge Injection (Note 9)	1.65 to 5.5				pC	C_L = 0.1 nF, V_{GEN} = 0V, R_{GEN} = 0 Ω, f = 1 MHz	Figure 3
OIRR	Off Isolation (Note 10)	1.65 to 5.5		-55.0		dB	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Figure 4
Xtalk	Crosstalk	1.65 to 5.5		−70.0		dB	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Figure 5
BW	−3dB Bandwidth	1.65 to 5.5		>300		MHz	R_L = 50 Ω	Figure 8
THD	Total Harmonic Distortion (Note 9)	5		.016		%	R_L = 600Ω 0.5 V_{P-P} f = 600 Hz to 20 KHz	

Note 8: This parameter is guaranteed by design. The switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance.

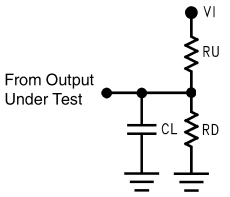
Note 9: Guaranteed by design.

Note 10: Off Isolation = 20 $\log_{10}$ [V_A/V_{Bn}]

Capacitance

Symbol	Parameter	Typ	Max	Units	Conditions	Figures
C_{IN}	Control Pin Input Capacitance	2.5		pF	V_{CC} = 0V	
$C_{I/O}$ (OFF)	Switch Port Off Capacitance	5.0		pF	V_{CC} = 5.0V	Figure 6
$C_{I/O}$ (ON)	Switch Port Capacitance when Switch is Enabled	10.0		pF	V_{CC} = 5.0V	Figure 7

AC Loading and Waveforms



Input driven by 50Ω source terminated in 50Ω

C_L includes load and stray capacitance.

Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit

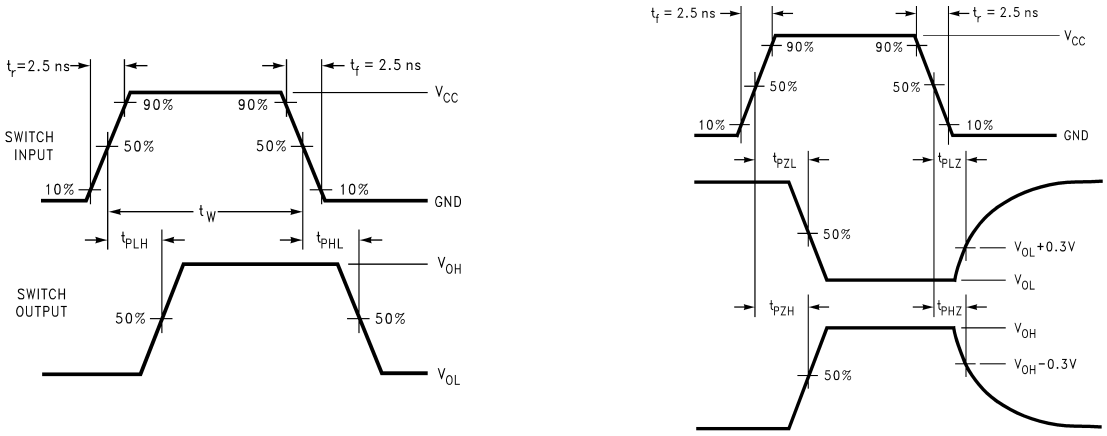


FIGURE 2. AC Waveforms

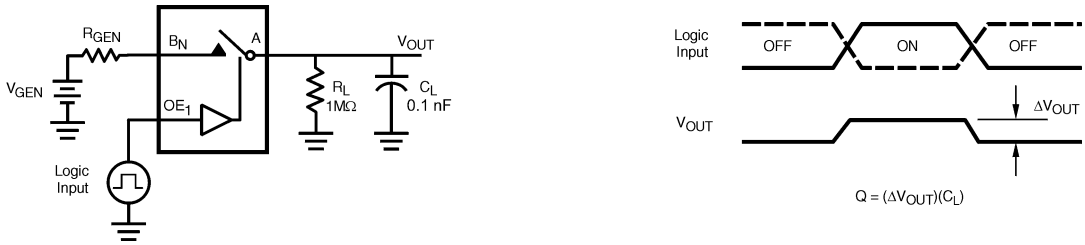


FIGURE 3. Charge Injection Test

AC Loading and Waveforms (Continued)

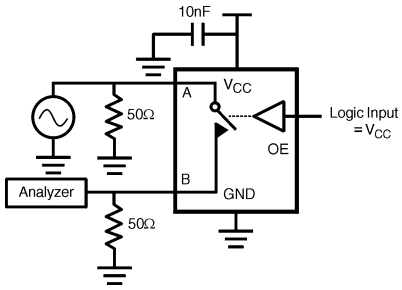


FIGURE 4. Off Isolation

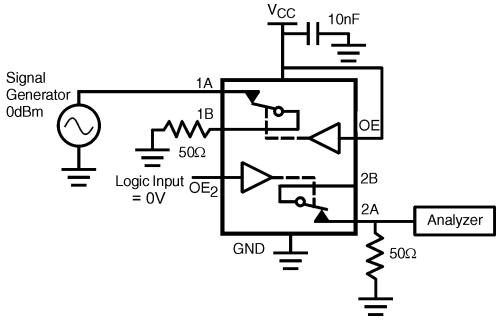


FIGURE 5. Crosstalk

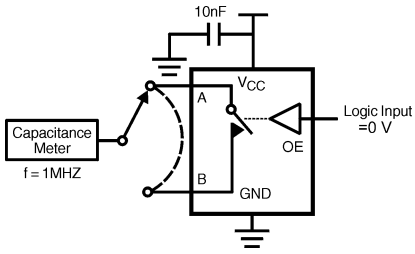


FIGURE 6. Channel Off Capacitance

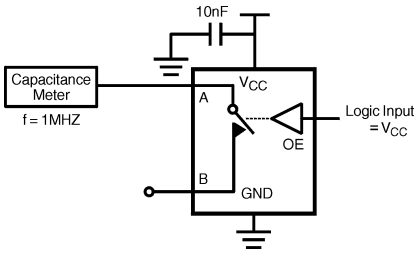


FIGURE 7. Channel On Capacitance

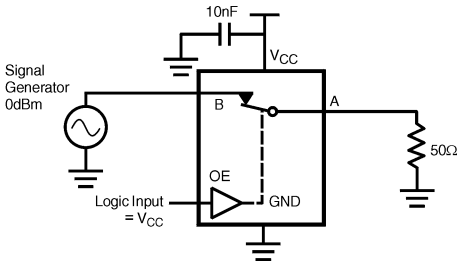


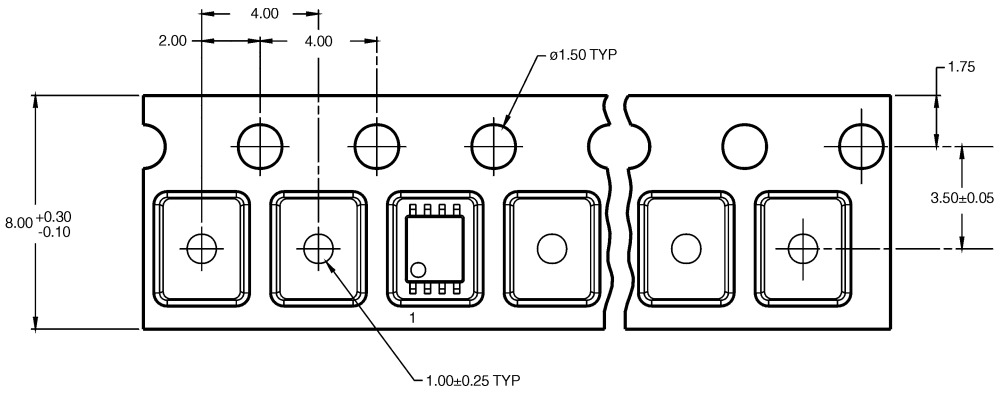
FIGURE 8. Bandwidth

Tape and Reel Specification

TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

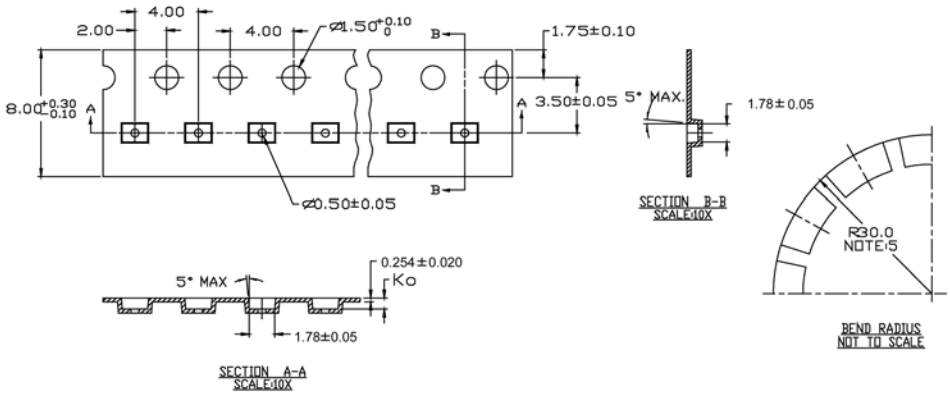
TAPE DIMENSIONS inches (millimeters)



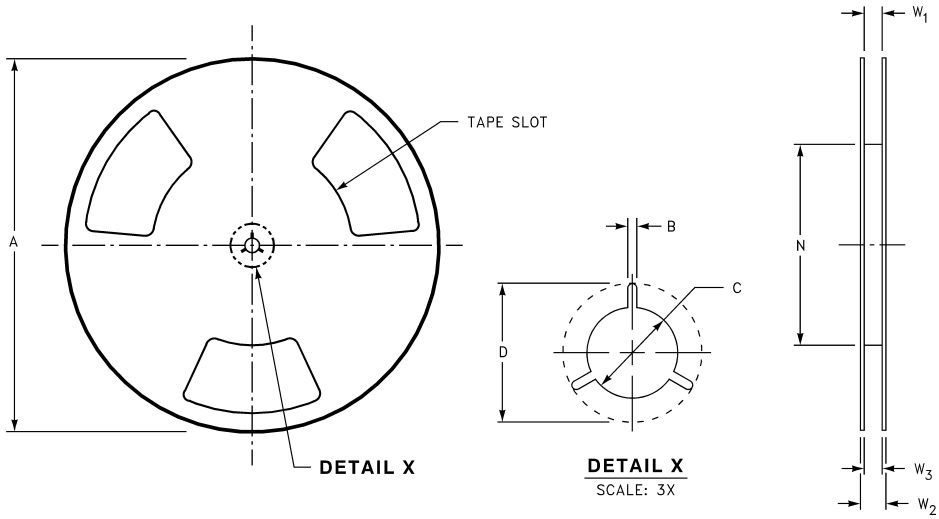
TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

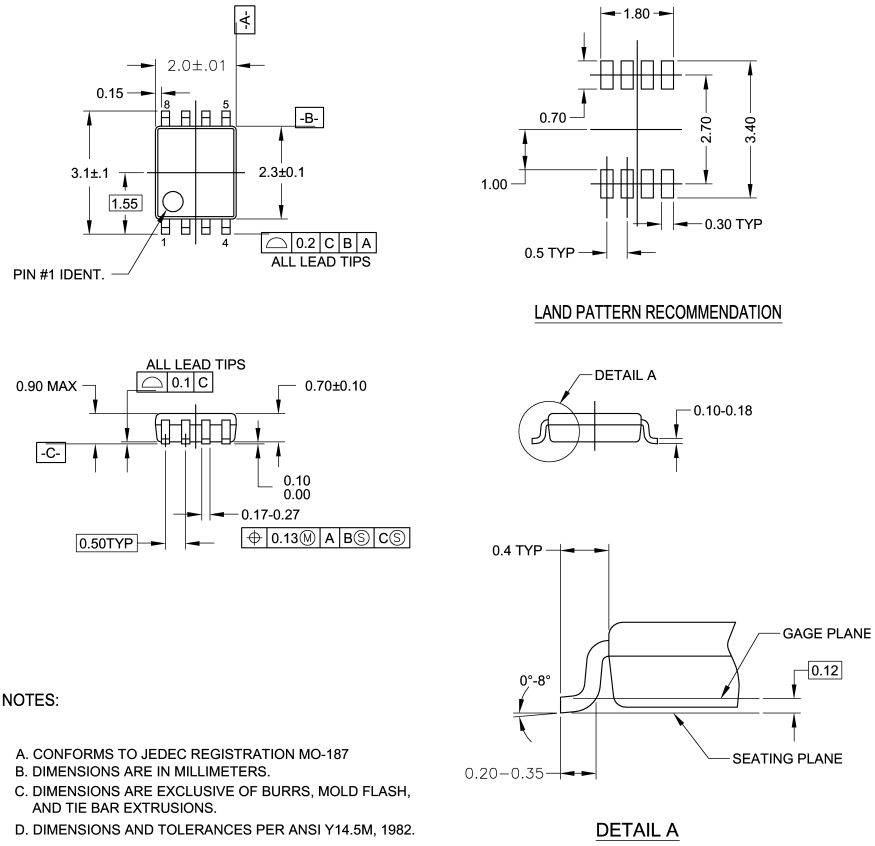


REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



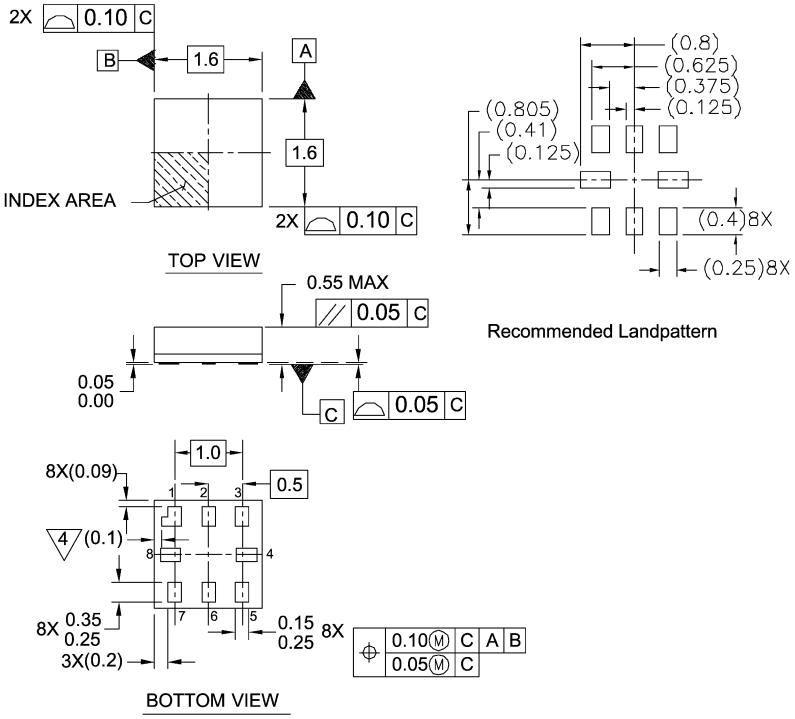
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

Pb-Free 8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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